REMARKS

The Applicant has filed the present Response in reply to the outstanding Official Action of September 8, 2004, and the Applicant believes the Response to be fully responsive to the Official Action for reasons set forth below in greater detail.

At the onset, the Applicant would like to note that Claims 1, 3-4, 6, 7-8, 10, 12, 13, 15, 21 (the second 21 mentioned in the specification), 23, 25, and 27-30 have been amended herewith to recite "a color display" instead of a "a color liquid crystal display" as "liquid crystal" has been removed.

Additionally, new Claims 39-55 have been added for examination in this application. New Claim 39 is directed to the method of Claim 1 further comprising the steps of generating a plurality of scanning signals by a scanning electrode driver circuit; applying sequentially said plurality of scanning signals to a plurality of scanning electrodes in the color display by controlling said scanning electrode circuit; applying sequentially data signals to said plurality of scanning electrodes by controlling a data electrode driving circuit. Claims 40-42 depend from Claim 39. Claims 40 and 41 contain limitations regarding the selection of the voltage level. Specifically, Claim 40 recites that voltages corresponding to highly significant bit signals of the image display data are selected to values which are high voltages different from a power voltage for driving the data electrode driving circuit or low voltages different from a grounded voltage and are applied to a corresponding data electrode as the data signals.

Claim 41 recites that if a reduction of power consumption is instructed, voltages selected based on highly significant bit signals of a digital image, which are high voltages different from a power voltage for driving the data electrode driving circuit or low voltages different from a grounded voltage is applied to a corresponding data electrode as the data signals.

Claim 42 recites that the highly significant bit signals are a plurality of most significant bits of the image display data. Claim 43 is dependant upon Claim 8 and is a corresponding circuit claim. Claims 44-48 are similar circuit claims to the method claims of Claim 40-42. Claim 49 is dependent on Claim 23 and is a corresponding portable device claim having similar subject matter to the circuit claim. Claims 50-54 depend either directly or indirectly from Claim 49.

New Claim 55 is direct to, *inter alia*, a method of driving a color liquid crystal display having a color liquid crystal display with a liquid crystal cell at each cross point of a plurality of scanning electrodes formed along with lines with a given distance, wherein generating a plurality of scanning signals by a scanning electrode driver circuit, the method comprising applying sequentially the plurality of scanning signals to a plurality of scanning electrodes in the color display by controlling the scanning electrode circuit; applying sequentially data signals to the plurality of scanning electrodes by controlling a data electrode driving circuit to drive the color liquid crystal display, applying a high voltage selected based on the highly significant bit signals of the digital image data, but different from power voltage for the driving, or a low voltage different

from the grounded voltage to the data electrode corresponding to the data signals if a reduction of power consumption is instructed; and applying a voltage for displaying "white" or "black" as the data signal regardless of the corresponding digital image data on an area of data electrode other than the area for display of the minimum necessary information is instructed on the color liquid crystal display.

New Claim 56 depends from Claim 8 and is directed to the structure of the data latch. No new matter has been added by these amends or new claims. Support can be found in Figures 14-16, pages 68-71, 81-82, 92-95.

New Claims 39-55 are patentably distinct from the cited references. The references fails to disclose at least (a) voltages corresponding to highly significant bit signals of the image display data are selected to values which are high voltages different from a power voltage for driving the data electrode driving circuit or low voltages different from a grounded voltage and are applied to a corresponding data electrode as the data signals; (b) voltages corresponding to highly significant bit signals of the image display data are selected to values which are high voltages different from a power voltage for driving the data electrode driving circuit or low voltages different from a grounded voltage and are applied to a corresponding data electrode as the data signals; and (c) applying a voltage for displaying "white" or "black" as the data signal regardless of the corresponding digital image data on an area of data electrode other than the area for display of the minimum necessary information is instructed on the color liquid crystal display.

In the outstanding Official Action, the Examiner rejected all of the claims of the application. Specifically, the Examiner rejected Claims 1-7 as being unpatentable over Chee et. al. (U.S. Patent No. 5,886,689) (hereinafter "Chee"). The Examiner asserts that Chee discloses a method of driving a LCD in both a normal drive mode and a power saving mode, wherein in the normal driving mode, the voltages corresponding to image display data are applied to data electrodes of the LCD and in the power saving mode, voltages corresponding to highly significant bit signals of the image data are applied as display data to the data electrodes. The Examiner admits that Chee fails to disclose that voltages to highly significant bit signals of the image display are applied as display data to the electrode however the Examiner contends that it would be obvious to one of ordinary skill in the art that Chee discloses this feature as Chee et al discloses that in different power saving modes, it is known to reduce voltages to non-significant items, such as changing from color to grey scale.

Applicant respectfully disagrees with the Examiner's rejection and traverses with at least the following analysis.

Chee discloses a VDC that has a power saving controller that implements several different power saving modes. Specifically, at column 1, the reference discloses a standard power conservation system for a laptop. The power management system allows the computer to be in any one of four states varying from on and active to on, sleep with power and/or a clock signal removed from certain units, to on and slow state which the

clock rate of the computer is reduced and finally an off state. See col 1, lines 43-65. Chee further discloses that a power saving controller has an interface with the LCD in order to facilitate such power saving functions as LCD back light off, LCD display off. See col 5, lines 37-48. The controller further includes a timer and a counter, for counting down a selected time interval of inactivity. The reference discloses four power saving modes, off, backlight turned off, reduce clock and reduced grey scale. In the reduced grey scale mode, the controller orders a grey scale image of a reduced level. This shift from a full palette image to an image of reduced grey scale level saves power, however, the user may not be able to perceive all parts of an image originally rendered in color.

The reference does not teach suggest or render obvious using the highest significant bits. Nor does the reference teach how to reduce the grey scale. At best, the reference suggests providing a two bit grey scale.

In stark contrast, the claimed invention uses the highest significant bits as data signals. An LCD control circuit 41 receives an input of a power saving mode signal PS, so that the control circuit 41 generates a color mode signal CM based on the power saving mode signal PS. The color mode signal CM is then supplied to the data electrode driver circuit 42.

In power saving mode, the power saving mode signal PS is in an activated level, and instructs the data electrode driver circuit 42 to save the power consumption. The

power saving mode signal PS in an inactivated level allows the data electrode driver circuit 42 to drive without saving the power consumption.

In the 8-color mode or power saving mode, other information than the contents, for example, month-and-day information, telephone numbers for calling, characters of e-mails, various marks such as a battery mark and an antenna mark are displayed in 8-colors on the color liquid crystal display 1.

The control circuit 43 receives a strobe signal STB, a polarity signal POL and a color mode signal CM from the control circuit 41. In the non-full-color mode or the 8-color mode, a switch control signal SWA is **inactivated**. In the full-color mode, the positive and negative switching signals Sswp and Sswn are activated to control the polarity selecting circuit 48 in operation. In the non-full-color mode or the 8-color mode, the positive and negative switching signals Sswp and Sswn are **inactivated**.

A data latch 44 supplies most significant bits MSB1, MSB2, -----, MSB528 of the display data PD'1, PD'2, ---- PD'528 to the output circuit 47, wherein the most significant bits MSB1, MSB2, -----, MSB528 are respective most significant bits of the 6-bits display data PD'1, PD'2, ---- PD'528. For example, the most significant bit MSB1 comprises 1-bit as the most significant bit of the 6-bits display data PD'1. The most significant bit MSB528 comprises 1-bit as the most significant bit of the 6-bits display data PD'528.

The gray scale voltage generating circuit 45 is responsible for operation in both normal and reduced power consumption mode. If a power saving mode signal PS is high level "H", then the driver circuit is in the power saving 8-color mode, wherein static and/or dynamic images are displayed in 8-color on the color liquid crystal display 1 of the mobile phone. The power saving mode signal PS is an externally supplied signal based on operation by use to the mobile phone. In the 8-color mode, the gray scale voltage generating circuit 45 is inactivated to display without using any gray scale.

In the 8-color mode, the polarity selecting circuit 48 is inactivated by always-fixed low levels of the positive and negative switching signals Sswp and Sswn, no gray scale voltages are outputted. In the 8-color mode, the switch 66-1 is always fixed at OFF by the switch control signal SWA, whereby no primary three color signal appears at the output node of the first output unit 47-1. In the 8-color mode, the second delayed color mode signal CM2 is low level "L", then the output control circuit 67-1 makes one of the p-channel MOS field effect transistor 68-1 and the n-channel MOS field effect transistor 69-1 turn ON and another turn OFF based on both the first delayed polarity signal POL1 and the most significant bit signal MSB1, whereby one of the power voltage VDD and the ground voltage GND is transmitted through the output node of the first output unit 47-1 to the data electrode of the color liquid crystal display 1. As described above, in the 8-color mode, the amplifier 65-1 is inactivated and no data red, green or blue color signal is supplied from the amplifier 65-1. In the 8-color mode, the predetermined high and low voltages are selectively applied to the data electrode for causing a predetermined large difference in rightness of the pixel. For this reason, it is possible to selectively apply a

different high voltage than the power voltage and another different low voltage than the ground voltage to the data electrode. In the 8-color mode, the second delayed color mode signal CM2 is low level "L", whereby the constant current circuit 70 is inactivated to generate no current. The most significant bit signals MSB1, MSB2, MSB3, ------, MSB528 ***are to be used only in the power saving 8-color mode***. Namely, in the full-color mode, ***the most significant bit signals MSB1, MSB2, MSB3, ——, MSB528 are not used.***

The display in the power saving mode is made in 8-colors, wherein the most significant bit signals are used. It is also possible that the display may be made in 16-colors or 32-colors in the power saving mode. In the 16-color mode, the most significant bit signals and second most significant bit signals are used. In the 32-color mode, the most significant bit signals, second most significant bit signals and third most significant bit signals are used.

Chee does not suggest using only the highest significant bits in power saving mode and not using the highest significant bits in normal power mode.

In addition, the present invention, includes selective inversions, based on the polarity signal POL, to the first to sixty fourth gray scale voltages V1, V2, V3, ----- V64 for every lines are made for allowing the non-inverted or inverted first to sixty fourth gray scale voltages V1, V2, V3, ----- V64 to be outputted. For this reason, each of the first to five hundred twenty eighth gray scale voltage selecting units 46-1, 46-2, 46-3, ----

-, 46-528 of the gray scale voltage selecting circuit 46 does not include any transfer gates, resulting in one half reduction in the number of the necessary elements for the gray scale voltage selecting circuit 46. The above one half reduction in the number of the necessary elements can reduce an occupied area over a printed board as well as can achieve a scaling down of the integrated circuit of the data electrode driver circuit 42 including the gray scale voltage selecting circuit 46, resulting in a certain reduction of chip size. The driver circuit as described above is thus suitable for various portable electronic devices

Chee does not suggest using a polarity signal to selective invert the gray scale voltages V1, V2, V3, ----- V64 for every lines are made for allowing the non-inverted or inverted first to sixty fourth gray scale voltages V1, V2, V3, ----- V64 to be outputted. In normal operation mode the data electrode is applied with data signals, wherein the data signals may include data red signals, data green signals and data blue signals, which have been generated from red data D_R, green data D_G, and blue data D_B as digital image data.

The color mode signal CM in an activated level, sets the data electrode driver circuit 42 in a full-color mode. The color mode signal CM in an inactivated level, sets the data electrode driver circuit 42 in a non-full-color mode, for example, an 8-color mode. In the full-color mode, various images such as static and/or dynamic images are displayed in full-colors on the color liquid crystal display 1.

In the 8-color mode, each pixel is displayed in 8-colors, wherein each pixel includes three-primary color dots, for example, red (R)-color dot, green (G)-color dot and

blue (B)-color dot, and each of the three-primary color dots, for example, red (R)-color dot, green (G)-color dot and blue (B)-color dot is displayed in binary digits.

The control circuit 43 also supplies color mode signal to the gray scale voltage generating circuit 45. The control circuit 43 also supplies the positive and negative switching signals Sswp and Sswn to the gray scale voltage generating circuit 45 and the polarity selecting circuit 48.

A data register 14 is supplied with display data PD1-PD528 which is then supplied to a data latch for voltage conversion into voltage converted 6-bits display data PD'1-PD'528 and further optionally performs, based on a polarity signal POL1, an inversion.

As shown in FIG. 15, each of the first to five hundred twenty eighth gray scale voltage selecting units 46-1, 46-2, 46-3, -----, 46-528 of the gray scale voltage selecting circuit 46 includes the p-channel MOS field effect transistors 62-1, 62-2, 62-3, ----- 62-32 on the high voltage side and also the n-channel MOS field effect transistors 63-1, 63-2, 63-3, ----- 63-32 on the low voltage side.
Furthermore, Chee does not teach any circuitry which accomplishes the reduced gray scale let alone the claimed circuits or features.

Lastly, Chee fails to teach that in the power saving mode, voltages corresponding to highly significant bit signals of the image display data are applied as the display data

signals to the data electrodes of the color liquid crystal display, in order to reduce the power ***consumption in the line-inversion driving system or the frame-inversion driving system.*** The present invention is capable of reducing the power consumption for drivers using both the line-inversion driving system and the frame-inversion driving system.

Accordingly, Chee fails to teach, suggest or disclose each and every limitation of the claim.

With regards to Claim 2, the Applicant respectfully disagrees with the Examiner's assertion that Chee discloses the a power saving mode that includes an essential information display mode, where a predetermined uniform voltage level is uniformly applied to all data electrodes on other regions that at least a designated region for displaying the essential information. First Chee fails to teach a designated region for displaying the essential information. Chee solely teaches reducing the gray scale level over the entire LCD. Second, the reference teaches that in the power reduction mode the user may not be able to perceive all parts of the image when the image is render in reduce gray scale. This teaches away from displaying essential information which is independent from the reduced gray scale or in other words. Thus, the reference fails to teach an essential information display mode, where a predetermined uniform voltage level, which corresponds to a predetermined color and which is independent from said image display data, is uniformly applied to all data electrodes on ***other region than at least a designated region for displaying the essential information.*** In the reference,

essential information may not be able to be perceived, whereas, in contrast, the user will be able to read the essential information.

In stark contract, the present invention allows for a partial display mode. The control circuit 81 receives a input of a partial display mode signal PI, so that the control circuit 81 generates a partial display signal PM, a monochrome signal BW and a plural scanning signal PC based on the partial display mode signal PI. The partial display signal PM, the monochrome signal BW and the plural scanning signal PC are then supplied to the data electrode driver circuit 82. The control circuit 84 receives a strobe signal STB, the polarity signal POL, the color mode signal CM, the partial display signal PM and the monochrome signal BW from the control circuit 41, so that the control circuit 84 generates a partial display signal PM1 and a monochrome signal BW1. This allows for part of the screen to be displayed in full color mode and part of the screen in partial color or power saving mode.

If both the power saving mode signal PS and the partial display mode signal PI are high-level "H", then this means that the mobile phone is in the stand-by mode, wherein a predetermined stand-by image is displayed on the color liquid crystal display 1. The control circuit 81 receives the power saving mode signal PS of high level "H" and the partial display mode signal PI of high level "H", based on which the control circuit 81 generates the color mode signal CM of high level "H", the partial display signal PM, and the monochrome signal BW of low level "L". The color mode signal CM of high level

"H", the partial display signal PM, and the monochrome signal BW of low level "L" are supplied to the data electrode driver circuit 82.

If the partial display signal PM is high level, then the switches 86-1a, 86-2a, 86-3a, -----, 86-528a turn OFF, while the switches 86-1b, 86-2b, 86-3b, -----, 86-528b turn ON. The 6-bits display data PD1, PD2, ---- PD528 outputted from the latch circuits 51-1, 51-2, 51-3, ----- 51-528 are not transmitted to the level shifters 52-1, 52-2, 52-3, ---- 52-528. The monochrome signal BW1 from the control circuit 84 is transmitted through the switches 86-1b, 86-2b, 86-3b, -----, 86-528b to the level shifters 52-1, 52-2, 52-3, ---- 52-528. Since the monochrome signal BW1 is low level "L", voltage conversion operations by the level shifters 52-1, 52-2, 52-3, ---- 52-528 unchange the monochrome signal BW1 at low level "L".

Figure 23 illustrates four possible examples of the combination of power saving mode and partial color mode. CMa signal indicates that the entire screen will be in power save mode, 8-color mode, CMb indicates that the entire screen will be in full color mode. CMc indicates that part of the screen will be in full color mode and part in power saving mode (top part) while CMd indicates that part of the screen will be in full color mode and the top and bottom of the screen will be in power saving mode.

In CMd, the center region of the display screen of the color liquid crystal display 1 displays "white" independent from the externally supplied red data D_R, green data D_G, and blue data D_B. Since the color liquid crystal display 1 is of the normally white type,

no voltages are applied to the data electrodes which correspond to the center region of the display screen of the color liquid crystal display 1. No voltage applications result in a desirable reduction of the power consumption.

Accordingly, the Applicant submits that Claim 2 is patentably distinct from Chee.

With regard to Claim 5, the Applicant respectfully disagrees with the Examiner for the same reasoning as applied to Claim 2. The reference fails to teach, "wherein a uniform scanning signal is simultaneously applied to all scanning electrodes on other region than said at least designated region for displaying the essential information". Furthermore, the Examiner cites Col 5, lines 37-48 and Col 5, line 66-col 6 line 12 as a teaching of this claim limitation. Additionally, the Applicant disagrees with the Examiner that the identified section teaches the claim limitation. Specifically, the cited sections teach that a reduced power can be achieved by having the LCD display off, a backlight off and other power saving features. The claimed power saving feature is neither suggested nor disclosed by the reference.

With regard to Claim 7, the reference fails to teach wherein said power saving mode further inactivates a gray scale voltage generating circuit, a polarity selecting circuit, and an output circuit included in a driver circuit for driving said color liquid crystal display. At best, the reference teaches reducing the gray scale voltage generating circuit output. However, there is no suggestion to inactivate it. Furthermore, the reference fails to teach a polarity selecting circuit, let alone, inactivating this circuit.

Therefore, the Applicant respectfully disagrees with the Examiner's rejection of the claim. The inactivation of the gray scale voltage generating circuit 45, the polarity selecting circuit 48 and the amplifiers 65-1, 65-2, 65-3, ---- 65-528 in the output circuit 47 during the power saving, 8-color mode results in a large reduction in power consumption by the driver circuit for driving the color liquid crystal display 1. The reference fails to teach inactivation of either the gray scale voltage generating circuit 45 or the amplifiers, the reference solely teaches reducing the gray scale level. Inactivation of the gray scale voltage generating circuit 45, the polarity selecting circuit 48 and the amplifiers 65-1, 65-2, 65-3, ---- 65-528 is not the only manner to reduce the gray scale level nor is only using the most significant bits.

The Examiner also rejected Claims 8-39 as being unpatentable over Isami et al. (U.S. Patent No. 6,166,725 (hereinafter "Isami") in view of Chee.

With regard to independent Claim 8, the hypothetically combined Isami and Chee system fails to teach a control circuit for inactivating said gray scale voltage generating circuit, the polarity selecting circuit, and said output the in a power saving mode, and also for applying voltages corresponding to highly significant bit signals of the image display data as display data signals to the data electrodes in the power saving mode. Applicant respectfully disagrees with the Examiner rejection of Claim 8 traverses this rejection for at least the same reasoning as applied above.

With regard to Claims 11 and 14, the Applicant respectfully disagrees with the Examiner rejection based upon at least the same argument as applied to Claim 2 and 5 respectively.

With regard to independent Claim 23, the hypothetically combined Isami and Chee system fails to teach a control circuit for inactivating the gray scale voltage generating circuit, the polarity selecting circuit, and the output circuit in a power saving mode, and also for applying voltages corresponding to highly significant bit signals of the image display data as display data signals to the data electrodes in the power saving mode for the same reasoning as Claim 1 and 8. Additionally, Claim 26 is patentably distinct from the cited references for the same reasoning as Claims 2 and 11. Further, Claim 29 is patentably distinct from the cited references for the same reasoning as Claims 5 and 14.

Claims 3-4, 6, 9-10, 12-13, 15-22, 24-25, 27-28, and 30-38 are patentably distinct from the cited references based their dependency from Claims 1, 8 and 23, respectively.

Lastly, the Applicant would like to note that Claim 21 has been given a new number, Claim 56, as the number 21 was repeated for two different claims. This amendment is simply an editorial correction.

For all the foregoing reasons, the Applicant respectfully requests the Examiner to withdraw the rejections of independent Claims 1-38 pursuant to 35 U.S.C. § 103(a).

Furthermore, the Applicant submits that new Claims 39-55 are in patentable form.

In conclusion, the Applicant believes that the above-identified application is in condition for allowance and henceforth respectfully solicits the Examiner to allow the application. If the Examiner believes a telephone conference might expedite the allowance of this application, the Applicant respectfully requests that the Examiner call the undersigned, Applicant's attorney, at the following telephone number: (516) 742-4343.

Respectfully submitted,

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